SON-1531

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of)
)
Yoshikazu KUROSE)
)
Serial No. 09/283,231) Group Art Unit: 2671
)
Filed: April 1, 1999) Examiner: M. PADMANABHAN
)
For: IMAGE PROCESSING APPARATUS)
AND METHOD OF PROCESSING)
IMAGES THAT STOPS OPERATION OF)
PIXEL PROCESSING CIRCUITS WHEN)
PIXEL DATA TO BE PROCESSED IS)
NOT NEEDED)

TRANSMITTAL OF REPLY BRIEF

Assistant Commissioner for Patents
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Washington, D.C. 20231

Sir:

Three copies of an Appellant's Reply Brief for the above-referenced application are being filed herewith. This Reply Brief is being timely filed in response to the Examiner's Answer dated July 22, 2002.

Respectfully submitted,

Dated: **September 23, 2002**

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In re the Patent Application of

Yoshikazu KUROSE

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For: IMAGE PROCESSING APPARATUS AND METHOD OF PROCESSING IMAGES THAT STOPS OPERATION OF PIXEL PROCESSING CIRCUITS WHEN PIXEL DATA TO BE PROCESSED IS NOT NEEDED

Group Art Unit: 2671

Examiner: M. PADMANABHAN

REPLY BRIEF

Assistant Commissioner for Patents
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This is a Reply Brief under Rule 193(b) in response to the Examiner's Answer (Paper No. 12) mailed on July 22, 2002. This Reply Brief is directed only to the new points of argument raised in the Examiner's Answer, as required by Rule 193(b).

I. NEW POINTS OF ARGUMENT

On pages 15 to 18 of the Examiner's Answer, the Examiner has set forth new points of argument in response to the arguments contained in the Appellant's Brief. Most of these new points of argument are believed to be adequately addressed in the Appellant's Brief and will not be further discussed herein. It is respectfully submitted that none of the Examiner's

remarks are persuasive to rebut the arguments previously set forth in the Appellant's Brief.

A. Kiyoto Does Not Teach Inhibiting a Clock Signal for Selected Pixel Processing Circuits Within a Block of Parallel Pixel Processing Circuits

On page 15 of the Examiner's Answer, the Examiner describes the processing blocks of Kiyoto as "devices, some of which are inhibited by image clock signal, and stopped from performing wasteful processing, when these devices do not receive image data." The Examiner goes on to state that the processing blocks of Kiyoto are similar to the parallel pixel processing circuits of the Appellant's claimed invention, which are also "devices." It is respectfully submitted that this new point of argument overlooks an important distinction between the Appellant's invention and the teachings of Kiyoto.

In the image processing device of Kiyoto, the image clock signal is inhibited for an entire processing block, and not just for selected pixels or pixel processing circuits within a processing block. There is no teaching or suggestion in Kiyoto that the operation of selected pixel processing circuits within a processing block should be stopped. Without this teaching, the teachings of Kiyoto have little relevance to the claimed invention.

The processing blocks of Kiyoto are not parallel pixel processing circuits. Instead, each of the processing blocks of Kiyoto is presumably made up of a plurality of parallel pixel processing circuits. In Kiyoto, if any one of the pixel processing circuits within the processing block have valid data, then the entire processing block will be considered as having valid data and will receive an image clock signal. If only one pixel processing circuit of a

processing block of Kiyoto has valid data, for example, and the processing block has seven other pixel processing circuits with invalid data, a large number of invalid operations will occur causing relatively high power consumption.

In contrast, the image processing apparatus of the present invention stops selected pixel processing circuits within a processing block when it is determined that those processing circuits are not needed for a particular image (e.g., they correspond to pixels outside a unit graphic).

It would not have been obvious to use the teachings of Kiyoto to modify the image processing method of Dawson et al. to inhibit a clock signal to at least one of a plurality of parallel pixel processing circuits that did not receive valid data. There is no teaching or suggestion in Kiyoto of stopping an image clock signal to selected pixel processing circuits of a plurality of pixels to be processed simultaneously (i.e., within a processing block), nor of stopping an image clock signal to a selected pixel processing circuit based on a judgment that the corresponding pixel is positioned outside a graphic unit to be processed. At most, Kiyoto might suggest modifying Dawson et al. to inhibit a clock signal to an entire processing block when none of the individual pixel processing circuits within the processing block have valid data. Such teachings are consistent with the related art image processing techniques described by the Appellant on pages 1 to 4 of the specification, and do not make the claimed invention obvious under 35 U.S.C. 103(a).

B. Dawson et al. Does Not Teach Stopping the Operation of the Pixel Processing Circuits for Pixels Outside the Unit Graphics

The Examiner states on page 15 of the Examiner's Answer that "It is inherent in Dawson that the pixels lying outside the polygon not be processed, since they would not be rendered." The Examiner further states on page 16 of the Examiner's Answer that "Dawson is relied on to teach a judgment that the corresponding pixel is positioned outside a graphic unit." The Appellant respectfully submits that these are new points of argument which are not persuasive for the following reasons.

Dawson et al. discloses a polygon rendering processing technique that generates image data across planar polygons by interpolating color, depth, elevation, and transparency from pixels on the edges of the polygon. In the polygon rendering technique performed by Dawson et al., processing is performed in parallel (simultaneously) for all pixels in a predetermined block. Since some of the pixels in a predetermined block fall outside the polygon being rendered and are not needed, the operations performed on these pixels become invalid. In Dawson et al., processing is performed on all of the plurality of pixels located in a predetermined block regardless of whether they are inside the polygon or not.

The Examiner's statement that the pixels lying outside the polygon in Dawson et al. are inherently not processed is incorrect and is not supported by any teachings in Dawson et al. or the other prior art of record. Indeed, the Examiner himself stated on page 5 of the Examiner's Answer that "Dawson . . . fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics." The Appellant agrees with

this latter statement by the Examiner.

As to the Examiner's argument that Dawson et al. teaches a judgment that the corresponding pixel is positioned outside a graphic unit, it is noted that Dawson et al. is silent as to whether such a judgment is made. The rendering engine 34 of Dawson et al. presumably calculates or interpolates both the interior and the exterior points, even though the calculated exterior points are considered invalid. There simply is no teaching in Dawson et al. of stopping an image clock signal or otherwise stopping the operation of selected pixel processing circuits within a block of parallel circuits based on a judgment that the corresponding pixel is positioned outside a graphic unit.

For these reasons and those stated on pages 9 to 13 of the Appellant's Appeal Brief, it is respectfully submitted that the combined teachings of Dawson et al. and Kiyoto would not have lead one of ordinary skill in the art to the Appellant's claimed invention.

C. Kiyoto Does Not Teach a Device for Use With "Polygon Rendering"

On page 15 of the Examiner's Answer, the Examiner states that Kiyoto deals with image processing devices and image processing means wherein pixel data is generated from image data input. The Examiner is apparently inferring that because Kiyoto deals with image processing devices that generate pixel data Kiyoto also teaches a device for use with "polygon rendering." This is a new point of argument and is incorrect.

As explained on page 9 of the Appeal Brief and on pages 1 and 2 of the

Appellant's specification, polygon rendering is an image processing technique used to express a 3-D model as a composite of polygons. In polygon rendering, image data is generated across each polygon by interpolating color, depth, elevation, transparency, etc. from pixels on the edges of the polygon. The image processing device of Kiyoto does not generate image data across polygons by interpolating color, depth, and so forth from pixels on the edges of the polygons. While the image processing device of Kiyoto can be used in digital copying machines and the like, it is not particularly suitable for 3-D computer graphics that rely on polygon rendering methods.

D. Huxley Does Not Teach a Judging Step That Controls Whether or Not the Pixel Processing Circuits Will Perform Blending

The Examiner states on page 16 of the Examiner's Answer that Huxley teaches a method in which a determination is made whether alpha blending will be performed. The Examiner further states that no blending would be performed in Huxley when the NoAlphabuffer bit is set, and that the AlphaBlendMode message provides for alpha blending. This new point of argument is not persuasive for at least the following reasons.

The image processing system of Huxley has an alpha blend unit that blends source color and destination color according to an alpha blend equation. If the alpha blend function is disabled, then the color message is passed through unchanged (column 61, lines 12 to 13, and lines 66 to 67).

Huxley also discloses that a NoAlphaBuffer bit can be included in the

AlphaBlendMode message. In this case, an alpha value of 1.0 is substituted (column 61, lines 38 to 40). Since an alpha value of 1.0 is used, it must be presumed that the pixel processing circuits continue to operate (using the alpha value of 1.0), even though alpha blending is not occurring. Thus, Huxley does not teach a system or method in which a determination is made whether alpha blending will be performed by the pixel processing circuits, and in which such a determination is used to stop pixel processing circuits that will not perform alpha blending.

E. Claims 18 and 37 Include a Limitation of Determining Whether to Perform a Rewrite of a Depth Data

On page 18 of the Examiner's Answer, the Examiner states that "determining whether to perform a rewrite of a depth data has not been claimed" in claims 18 and 37. This statement is incorrect.

Claims 18 and 37 depend upon respective independent claims 17 and 36, both of which include a control circuit or step for judging whether or not to rewrite third pixel data corresponding to second depth data. These limitations of claims 17 and 36 are by definition included in claims 18 and 37 and provide a circuit or step for determining whether to perform a rewrite of a depth data. As such, claims 18 and 37 clearly support the Appellant's position that Huxley does not teach or suggest the claimed system or method in which a clock signal is stopped after determining not to perform a rewrite of depth data.

II. CONCLUSION

It is respectfully submitted that the final rejections of claims 1 to 40 are improper and should not be sustained for these additional reasons. Therefore, a reversal of the final rejections of the Examiner is again respectfully requested.

Respectfully submitted,

Dated: **September 23, 2002**

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